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Design and Simulation of an Improved Phase-Shifted Full-Bridge DC-DC Converter with Lower RMS Current and Voltage Stresses

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Abstract: In this paper, an improved phase-shifted full-bridge (PSFB) dc-dc converter with coupled inductors and a current doubler rectifier (CDR) circuit is proposed for battery charger applications in electric vehicles (EVs). By using two inductors, coupled with the traditional output filter inductors, the RMS currents, the circulating currents, and the voltage stresses on the converter secondary side are decreased. Also, the converter zero-voltage-switching (ZVS) operation range and its efficiency are improved, as well. The included coupled inductors at the primary side are small and have negligible values, as compared to the output inductors. Consequently, cost and size of the converter are not increased, as compared to the traditional one. For the conventional PSFB converter with a single inductor at its output filter, only a single coupled inductor is used and the same results are obtained, as investigated, here. Also, the conventional control system can be used easily, here. Moreover, the necessary current value for ZVS operation of the power MOSFETs is decreased which improves the converter efficiency over a wider load variation ranges. Finally, to verify the given converter benefits, both proposed and traditional converters have been simulated under the following conditions: input voltage (*150-250 V*), switching frequency (*200 kHz*), output voltage (*75-85 V*), and the output current (*1.85-18.5 A*). The given results clearly show major improvements in the proposed converter efficiency and currents and voltages stresses over the traditional one.

Key words: Battery Charger, Circulating Current, Current Doubler Rectifier, Phase-Shifted Full-Bridge DC-DC Converter, Zero-Voltage-Switching (ZVS).

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1. introduction

Due to greenhouse effects, decreasing natural resources,[1] and air pollution, fossil fuels can adversely affect the environment. The aforesaid major drawbacks give rise to the widespread use of electric vehicles. Compared with conventional internal-combustion engine vehicles, the EVs have some major benefits; high efficiencies, less involvement in environmental problems, and more safety equipments, for instance [1]. Due to the fact that the battery chargers play an absolutely crucial role in the EV system, the chargers must have some features such as high efficiencies, high reliability, low electromagnetic interference (EMI), and fast charging capability [2, 3]. Lithium-Ion cells are widely used in EVs with high voltage batteries. Fig .1 shows the charging processes of a single lithium-ion cell [4-6]. Based on this figure, during the charging process a wide output voltage range is needed. Consequently, the battery charger must experience high efficiency from light loads to full loads to guarantee the long lifespan of the batteries and prevent safety damages. As a result of some major benefits including low EMI, high power density, and high power efficiency, the PSFB dc-dc converter is widely employed in battery chargers [3-9].

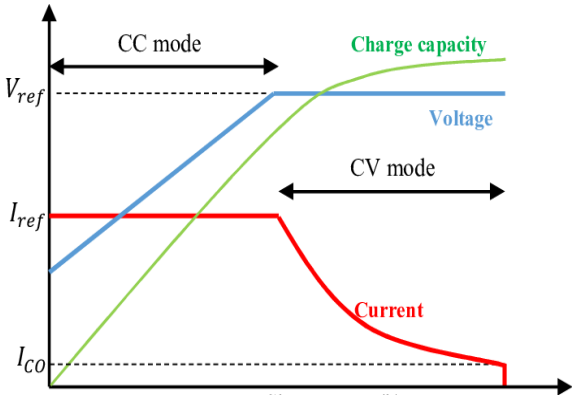


Fig. 1 Charging profile of a single lithium-ion cell [4, 5].

By using the CDR at the converter output side, low charging current ripple and low current rating values at the transformer secondary side windings are obtained. Consequently, reliability and efficiency of the charger is [2]improved for high output current applications. To achieve ZVS operation of the converter power MOSFETs and zero-current-switching (ZCS) operation of its output power diodes, multiple structures and methods have been proposed [9-21]. The phase-shift control strategy is the well-known and most convenient method which is employed for obtaining the ZVS operation in full-bridge dc-dc converters. In addition to its major benefits, PSFB dc-dc converter suffers from some drawbacks including losing the ZVS operation under the light load conditions which is vital for the chargers and leads to high EMI noises, high switching losses, high voltage stresses on the secondary side components, and significant power dissipation, due to circulating currents during the freewheeling interval [4, 9].

To overcome the aforementioned drawbacks, several topologies and control strategies have been proposed in litreture. To improve the ZVS operation range of the power MOSFETs for wider load variations ranges, some converters with auxiliary circuits have been proposed, too [10-13]. But, some extra components are needed which results in higher cost and size, due to the presence of the auxiliary circuits. Besides, the currents stresses on the primary side are increased which decrease the converter reliability and efficiency. To eliminate and reduce voltage spikes on the converter secondary side components, several topologies with active clamps have also been given by researches [14-17]. Due to presence of the active clamps, some extra components are required which increase volume and costs of the converters, as mentioned recently. In addition, some power dissipation is occurred in the active clamps which reduces the efficiency. To reduce or eliminate the circulating currents, several topologies with different control strategies such as hybrid full-bridge dc-dc converter and secondary side PSFB dc-dc converters have been proposed, too [18-23]. Although, these converters can decrease or completely overcome the circulating currents, but they suffer from higher cost and size because of extra passive and active components.

Here, an improved PSFB dc-dc converter with two output coupled inductors and a CDR circuit is proposed with the aim of reducing the RMS currents, the secondary side voltage stresses, the circulating current, and to extend the ZVS operation range of the power MOSFETs. By using the coupled inductors instead of conventional filter inductors, the overall efficiency from light load to full load is increased, significantly. Furthermore, by decreasing the voltage stresses and spikes on the secondary side, a more reliable system is obtained. Due to the fact that there are no particular and complex control strategy or auxiliary circuits in the proposed improved PSFB battery charger, the proposed converter is relatively simple and benefits from low size and cost, as compared with other PSFB dc-dc converters. It must be mentioned that for the conventional PSFB converter with a single inductor at its output filter, only a single coupled inductor can be used and the same results are obtained, as investigated here, in detail.

The proposed improved PSFB dc-dc converter with coupled inductors and a CDR circuit is introduced in Section II. Operational principles and design considerations of the proposed converter are

described in Section III. A complete comparison between the proposed improved PSFB dc-dc converter and the conventional one and also their simulation results are given in Sections IV and V, respectively. . Finally, the conclusion is drawn in Section VI.

2. Proposed Improved PSFB DC-DC Converter with Two Coupled Inductors and a CDR Circuit

The proposed improved PSFB dc-dc converter with two coupled inductors and the CDR circuit is shown in Fig .2. By switching the power MOSFETs ($Q_1 - Q_4$), a square voltage waveform is generated on the main transformer primary side to regulate the output current and the output voltage during constant current (CC) charging and constant voltage (CV) charging processes, respectively. By employing the CDR circuit at the main transformer secondary side, the currents ratings of the main transformer secondary windings are decreased. Therefore, in the applications where the output current, in this case during the CC charging interval, the overall efficiency is boosted [6]. In the conventional PSFB dc-dc converter with the CDR at the output side, the ZVS operation for the power MOSFETs by utilizing the leakage inductance (L_{lkg}) and the MOSFETs drain-source capacitors (C_{ds}) is achieved. The required energy for the ZVS operation is tightly related to the leakage inductance value. By increasing the leakage inductance value, the required current for the ZVS operation is reduced but, this leads to higher voltage spike and stresses on the secondary side, more noise, and lower gain at the output port. It is noteworthy to mention that, by inverting the recursive inductors dots in the proposed improved converter, as shown in Fig. 2, the efficacy of the two coupled inductors on the converter performance including the RMS currents reducing, the voltage stresses reducing, and extending the ZVS operation range of the power MOSFETs, are degraded, dramatically.

3. Operational Principles and Design Considerations

3.1. Operational Principles

The key voltages and currents waveforms of the proposed converter are shown in Fig. 3. D and f_s are duty cycle and switching frequency, respectively. By changing the phase-shift time between two different legs, the output voltage and current are adjusted. During the charging operation, the duty cycle is kept constant, to simplify the analyses, and for better understanding the object, the following assumptions have been taken, too:

- The proposed PSFB dc-dc charger operates under the steady state condition.
- The output capacitor equivalent-series-resistor (ESR) is ignored.
- All semiconductor switches including the power MOSFETs and diodes are non-ideal.

Different operation modes and equivalent circuits of each mode are depicted in Fig. 4, in sequence, and they are described in detail, as follows:

Mode 1: ($t_0 - t_1$): During this operation mode, as shown in Fig. 4, the primary current (i_p) is negative. The main transformer primary side voltage can be

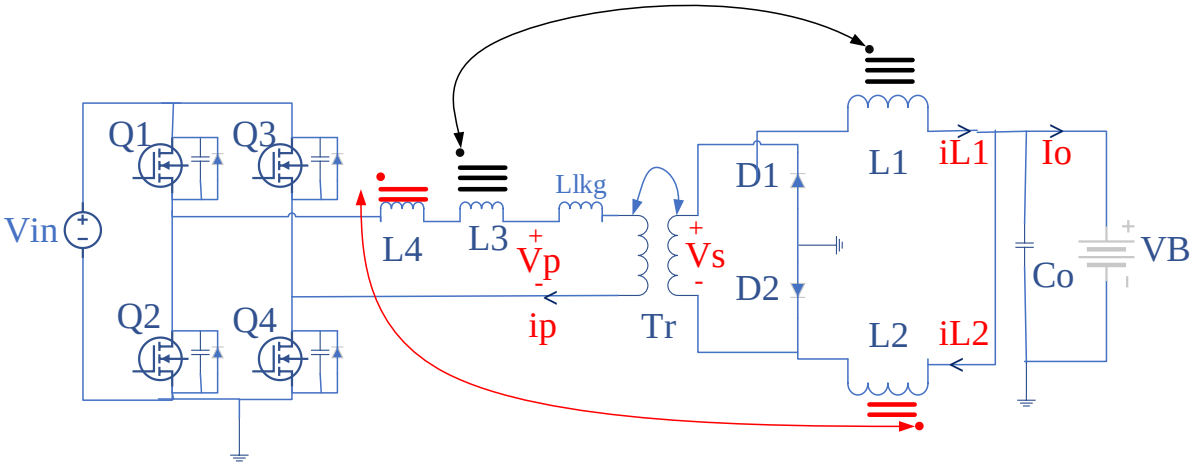


Fig. 2 Proposed improved PSFB dc-dc converter with two coupled inductors and a CDR circuit for battery charger applications.

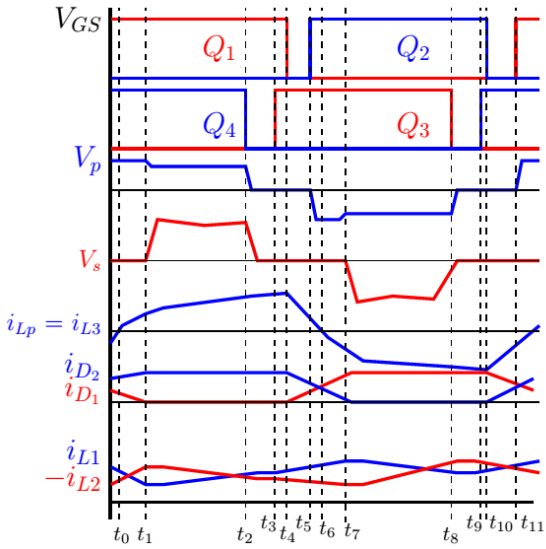


Fig. 3 The key voltage and current waveforms of the proposed charger.

expressed as follows:

$$v_p(t-t_0) = -V_{in} - v_{L3}(t-t_0) - v_{L4}(t-t_0) \quad (1)$$

The transformer primary current and the output inductors currents are also given by

$$\begin{cases} i_p(t-t_0) = i_{L3}(t-t_0) = -\dfrac{v_p}{L_{Lkg}+L_T} \times (t) \\ i_{L1}(t-t_0) = -\dfrac{V_B}{L_1} \times (t) + I_{L1}(t_0) \\ i_{L2}(t-t_0) = \dfrac{V_B}{L_2} \times (t) + I_{L2}(t_0) \end{cases} \quad (2)$$

where $L_T = L_3 + L_4$, and $I_{L1} - I_{L2}$ are the initial values of i_{L1} and i_{L2}, respectively. When primary current is positive this state is ended.

Mode 2: $(t_1 - t_2)$: During this operation state, the primary current is positive and Q_1 and Q_4 are both on. Consequently, D_2 at the secondary side is turned on and the power is transferred to the batteries. During this operation mode, i_{L1} is reduced and v_{L4} is increased. The primary and the two recursive inductors voltages are given by Eq. (3):

$$\begin{cases} v_p(t-t_1) = -V_{in} - v_{L3}(t-t_1) - v_{L4}(t-t_1) \\ v_{L3}(t-t_1) = -\dfrac{V_B}{n_2} \\ v_{L4}(t-t_1) = -\dfrac{V_B + n_1 v_p(t)}{n_3} \end{cases} \quad (3)$$

Also, the output inductors currents are given easily.

$$\begin{cases} i_{L1}(t-t_1) = -\dfrac{V_B}{L_1} \times (t) + I_{L1}(t_1) \\ i_{L2}(t-t_1) = -\dfrac{(V_B + n_1 v_p(t))}{L_2} \times (t) + I_{L2}(t_1) \end{cases} \quad (4)$$

Where, n_1, n_2, and n_3 are turn-rations of the main transformer and output coupled inductors, respectively. This state is finished when Q_4 is switched off by the controller.

Mode 3: $(t_2 - t_3)$: The equivalent circuit of this operation mode is shown in Fig. 4(c) According to this figure, when Q_4 is turned off, the drain-source capacitor of Q_4 is charged from 0 to $(V_{in} - v_{L3} - v_{L4})$ and the drain-source capacitor of Q_3 is also discharged from $(V_{in} - v_{L3} - v_{L4})$ to 0 volts. The primary current and voltage can easily be expressed as:

$$i_p(t-t_2) = -n_3 i_{L2}(t-t_2) - n_2 i_{L1}(t-t_2) \quad (5)$$

$$v_p(t) = (V_{in} - v_{L3}(t-t_2) - v_{L4}(t-t_2) - v_{CQ4} \quad (6)$$

The drain-source capacitors voltage is given by

$$\begin{aligned} v_{CQ3}(t-t_2) &= V_{in} - v_{L3} - v_{L4} - \frac{n_3 i_{L3}(t) - n_2 i_L}{2C_Q} \\ v_{CQ4}(t-t_2) &= -\frac{n_3 i_{L3}(t) - n_2 i_{L1}(t)}{2C_Q} \end{aligned} \quad (7)$$

Mode 4: $(t_3 - t_4)$: When $v_{CQ3}(t)$=0, then the body diode of the Q_3 is turned on and its ZVS operation condition is realized. To ensure the ZVS operation of Q_3, a proper dead-time interval between Q_3 turning on and Q_4 turning off moments is needed. This required dead-time value is calculated as follow:

$$T_{d-lead} = \frac{4C_Q\left(V_{in} - v_{L3}(t_3) - v_{L4}(t_3)\right)}{n_3 i_{L3}(t_3) - n_2 i_{L1}(t_3)} \quad (8)$$

The primary current and voltage values during this interval can be calculated as below:

$$i_p(t-t_3) = n_1 i_{L1}(t-t_3) \quad (9)$$

$$v_p(t-t_3) = -v_{L3}(t-t_3) - v_{L4}(t-t_3) \quad (10)$$

Also, the output inductors currents can be given by:

$$\begin{cases} i_{L1}(t-t_3) = -\dfrac{V_B}{L_1} \times (t) + I_{L1}(t_3) \\ i_{L2}(t-t_3) = \dfrac{V_B + n_1 v_p(t)}{L_2} \times (t) + I_{L2}(t_3) \end{cases} \quad (11)$$

when Q_1 is switched off, this operation mode is finished.

Mode 5: $(t_4 - t_5)$: Fig. 5(e) shows the equivalent circuit of this state. By the time $t = t_4$ and once the Q_1 is turned off, the stored-energy in the main transformer leakage inductance and the two recursive inductors is discharged through the drain-source capacitor of the Q_1. The previous capacitor is charged from 0 to $(V_{in} - v_{L3} - v_{L4})$ and the drain-source capacitor of the Q_2 is discharged vice versa. The primary current is expressed as below:

$$i_p(t-t_4) = n_3 i_{L3}(t-t_4) - n_2 i_{L1}(t-t_4) \quad (12)$$

The output inductors current can be expressed by Eq. (13):

$$\begin{cases} i_{L1}(t-t_4) = -\dfrac{V_B}{L_1} \times (t) + I_{L1}(t_4) \\ i_{L2}(t-t_4) = \dfrac{V_B}{L_2} \times (t) + I_{L2}(t_4) \end{cases} \quad (13)$$

when the drain-source capacitor of the Q_2 is completely discharged, this state is finished.

Mode 6: $(t_5 - t_6)$: During this operation state, the body diode of the Q_2 is turned on. Then, similar to the mode 4, the ZVS operation of the Q_2 is obtained.

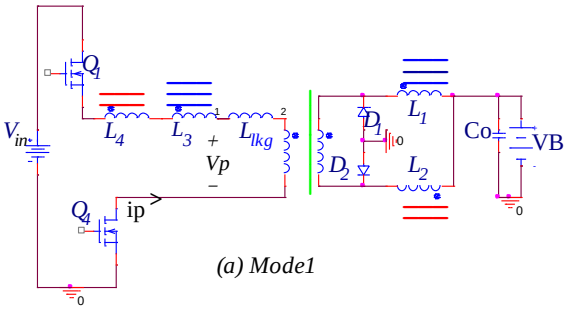
To ensure the ZVS operation of the Q_2, a decent dead-time between the Q_2 turning on and the Q_1 turning off is needed. This required proper dead-time is given by:

$$T_{d-lag} = \frac{4C_Q\left(V_{in} - v_{L3}(t_5) - v_{L4}(t_5)\right)}{n_3 i_{L3}(t_5) - n_2 i_{L1}(t_5)} \quad (14)$$

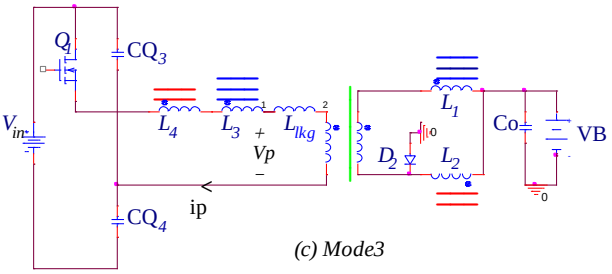
During this operation mode, the primary current is expressed as follow:

$$i_p(t - t_5) = -\frac{v_p}{L_{lkg} + L_T} \times (t) \quad (15)$$

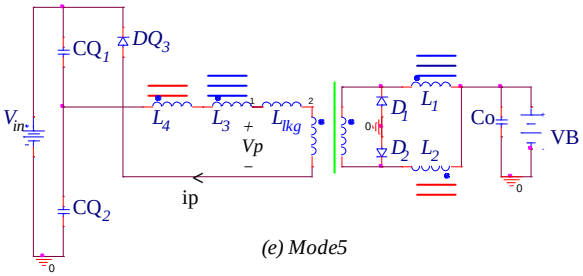
According to Fig. 3 and Fig. 4, the proposed converter has symmetrical waveforms and operation states. Therefore, the operation principle of the proposed improved converter during modes 7-12 is similar to modes 1-6 and, as a result, the converter analysis remains the same as discussed during modes 1-6.



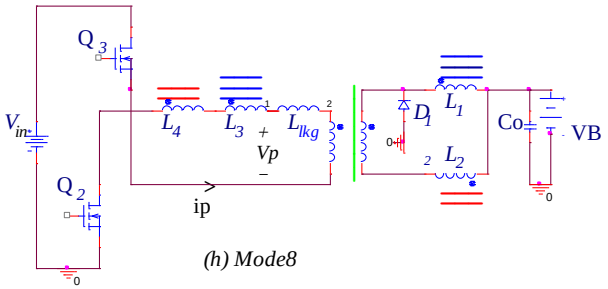
(a) Mode1



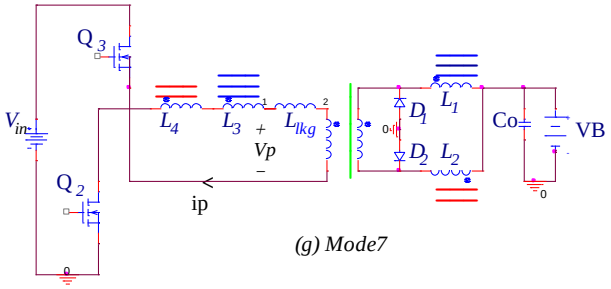
(c) Mode3



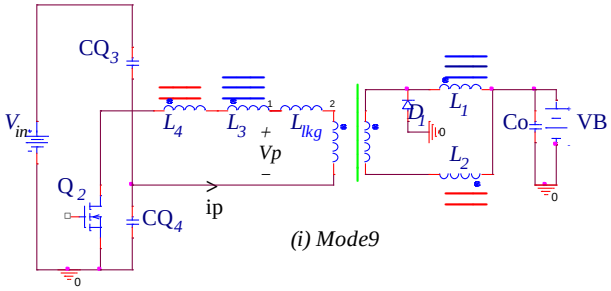
(e) Mode5



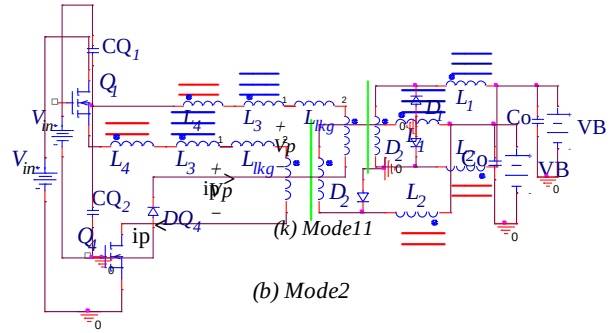
(h) Mode8



(g) Mode7

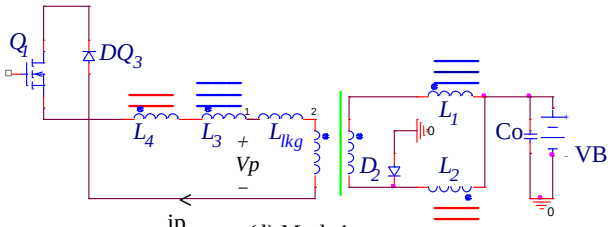


(i) Mode9

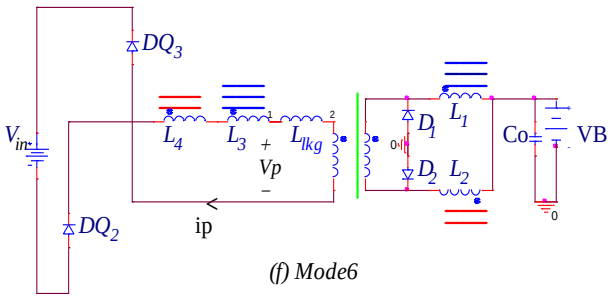


(k) Mode11

(b) Mode2



(d) Mode4



(f) Mode6

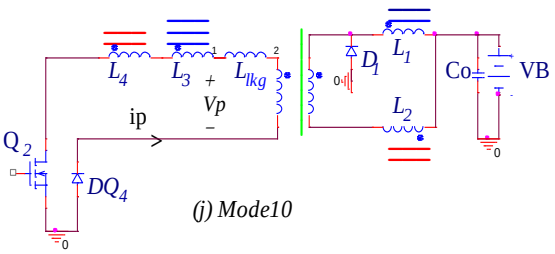


Fig. 4 Different operation modes of the proposed improved PSFB charger.

Therefore, to guarantee the ZVS operation, the stored-energy in leakage inductance and two recursive inductors must be greater than the energy-stored in the leg drain-source capacitors. Thus,

$$E_L > E_{Cleg} \quad (19)$$

By substituting Eq. (16) and Eq. (17) in Eq. (19), we can write

$$L_{lkg} + L_T > \frac{C_{leg}}{i_{p,min}^2}(V_{in.max} - v_{L3} - v_{L4})^2 \quad (20)$$

The Eq. (20) is used to select the proper leakage inductance of the main transformer to ensure the ZVS operation of power MOSFETs by using the phase-shift control method in proposed improved PSFB dc-dc converter with two coupled inductors and the CDR.

3.3. Design Considerations

The main parameters for designing the proposed converter are tabulated in Table I.

Table 1 Proposed Improved PSFB Charger Key Parameters.

Description	Symbol	Value
Input Voltage Range	$V_{in.min}$-$V_{in.max}$	150-250 V
Batteries Voltage Range	V_B	75-85 V
Constant Current Charging	I_{CC}	18.5 A
Maximum Output Power	$P_{out,max}$	1400 W
Output Capacitor Ripple	ΔC_o	50 mV
Output Current Ripple	ΔI_o	0.4 A
Duty Cycle	D	0.42
Switching Frequency	f_{sw}	200 kHz

The main transformer second side voltage is calculated as follow:

$$V_s = \frac{V_{B,max}}{D} = 200\ V \quad (21)$$

The main transformer turn-ratio is given by

3.2. ZVS Condition

To ensure the ZVS operation of power MOSFETs, the energy-stored in leakage inductance and two recursive inductors should discharge the drain-source capacitors. The aforementioned energy can be expressed as below:

$$E_L = \frac{L_{lkg} + L_T}{2} i_p^2 \quad (16)$$

The stored-energy in drain-source capacitors of each leg is given by

$$E_{Cleg} = \frac{C_{leg}}{2}(V_{in} - v_{L3} - v_{L4})^2 \quad (17)$$

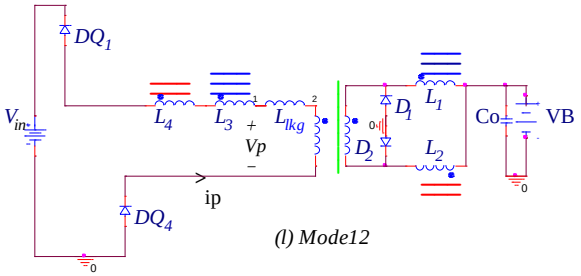
Where,

$$C_{leg} = C_{Q1} + C_{Q2} = C_{Q3} + C_{Q4} = 2C_Q \quad (18)$$

$$n_1 = \frac{N_s}{N_p} = \frac{V_s}{V_{in.min} - v_{L3} - v_{L4}} = \frac{200}{120} = 1.67 \quad (22)$$

The main transformer magnetizing inductance is calculated by Eq. (23):

$$L_m = \frac{(V_{in.min} - v_{L3} - v_{L4}) \times D \times T_s}{\Delta I_o \times n_1} \approx 370\ \mu H \quad (23)$$



The output filter inductors are given by

$$L_1 = L_2 = \frac{T_s \times V_{B,max} \times (1 - D)}{2\Delta i_L} \approx 101\ \mu H \quad (24)$$

The output filter capacitor is given by

$$C_o = \frac{T_s \times D \times \Delta i_L}{\Delta v_o} = 100\ \mu F \quad (25)$$

Finally, the recursive inductors are calculated by Eq. (26):

$$L_3 = L_4 = \frac{T_s \times V_{L3} \times D}{\Delta i_{L3}} = \frac{5 \times 15 \times 0.42}{24} \approx 1.5 \mu H \quad (26)$$

4. Comparison between the Proposed Improved PSFB DC-DC Converter and the Conventional One

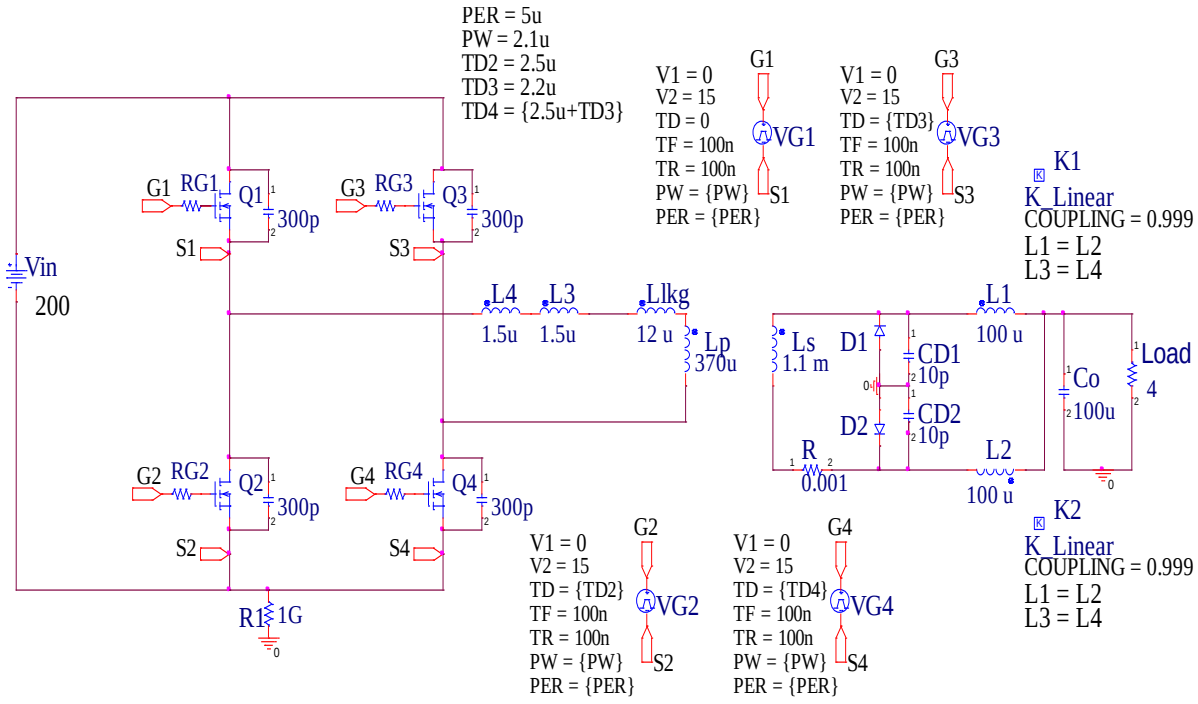
The traditional PSFB dc-dc converter with the CDR was proposed in [8]. According to this reference, the drain-source capacitors in the traditional converter are discharged from V_{in} to 0 volts. But the aforesaid capacitors are discharged from $(V_{in.min} - v_{L3} - v_{L4})$ to 0 volts, in the proposed converter in this paper. Consequently, the required energy for the ZVS operation of the power MOSFETs is decreased. In addition, more energy is stored in the proposed improved PSFB charger by employing $L_T + L_{lkg}$ compared with conventional PSFB converter. Therefore, the ZVS operation range is

extended. The RMS currents are significantly reduced in the proposed charger, hence higher efficiencies, and a more reliable system compared to the traditional PSFB converter is achieved. The voltage stresses and oscillation are significantly decreased in the proposed charger as opposed to the traditional PSFB converter. As a result, the efficiency, and the reliability of the proposed charger are increased and the total cost is reduced. In the traditional PSFB dc-dc with the CDR experiences simultaneous conduction performance of the output diode rectifiers in eight states. But, in the proposed improved PSFB dc-dc converter with two coupled inductors and the CDR, the simultaneous conduction performance of the output diode rectifiers in six states and less time is established. Therefore, lower circulating currents and higher efficiencies are obtained. The aforementioned benefits, make the proposed converter a suitable converter for EV battery charger applications.

5. Simulation Results

To give a better understanding and indicate the major advantages of the proposed improved PSFB dc-dc converter with two coupled inductors and the CDR over the conventional PSFB dc-dc converter with the CDR [8], both converters have been simulated by PSpice. The key parameters of both proposed and conventional converters are given in Table 2. The simulated circuits of the proposed and the traditional converters are depicted in Fig. 5 and Fig. 6, respectively. The applied pulse signals to the power MOSFETs gates are non-ideal and have fall-time and rise-time values equal to 100 ns. The simulation is done for two different conditions: nominal load with the nominal input voltage, and light load with the maximum input voltage.

Fig. 5 The simulated circuit of the proposed improved PSFB dc-dc charger in the PSpice .



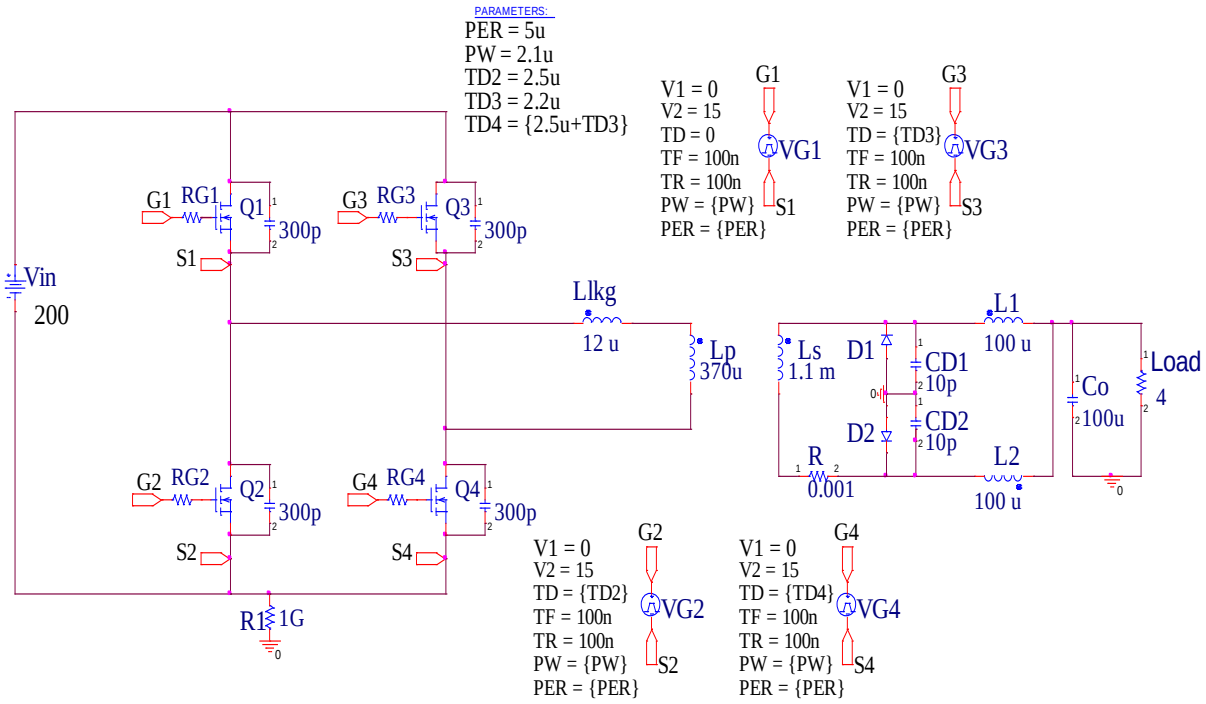


Fig. 6 The simulated circuit of conventional PSFB with the CDR converter in the PSpice.

Table 2 Key Parameters of Both Converters for Simulation in PSpice Software.

Description	Parameter	Value	
		Proposed Converter	Traditional Converter
Input Voltage Range	$V_{in.min}$-$V_{in.max}$	150-250 V	150-250 V
Batteries Voltage Range	$V_{B,min}$-$V_{B,max}$	75-85 V	75-85 V
Constant Current Charging	I_{CC}	18.5 A	18.5 A
Constant Voltage Charging	V_{CV}	85 V	85 V
Maximum Output Power	$P_{out,max}$	1400 W	1400 W
Recursive Inductors	L_3=L_4	1.5 µH	---
Output Inductors	L_1=L_2	101 µH	101 µH
Magnetizing Inductor	L_m	370 µH	370 µH
Leakage Inductor	L_{lkg}	5 µH	5 µH
Dead-Time	T_{dead}	200 ns	200 ns
Switching Frequency	f_{sw}	200 kHz	200 kHz
Coupled Inductors Turn-Ratios	n_2=n_3	8.17	---
Main Transformer Turns Ratio	n_1	1.67	1.67
Output Filter Capacitor	C_o	100 µF	100 µF
MOSFETs	Q_1-Q_4	IRFP460	IRFP460

The power MOSFETs currents and voltages under the nominal load and the nominal input voltage are shown in Fig. 7. According to this figure, the ZVS operation for all power MOSFETs is obtained. Besides, the power MOSFETs currents and voltages under the light load and the maximum input voltage are shown in Fig. 8 which delineates the ZVS operation for all power MOSFETs has been achieved.

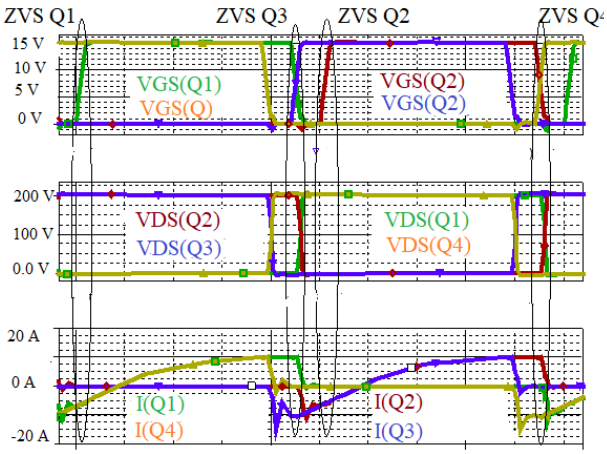


Fig. 7 The voltages and currents of the power MOSFETs in the proposed charger under the nominal load and nominal input voltage condition.

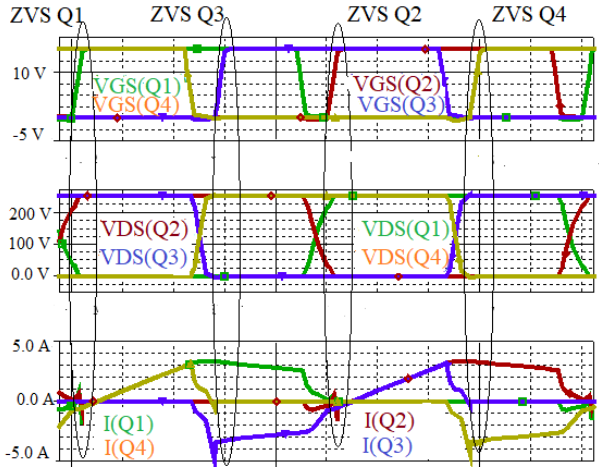


Fig. 8 The voltages and currents of the power MOSFETs in the proposed charger at light load and the maximum input voltage.

Fig. 9 shows the primary and secondary currents in the proposed improved PSFB dc-dc charger and the conventional PSFB dc-dc converter, respectively. According to Fig. 9, the proposed improved PSFB dc-dc charger has lower RMS currents, approximately 3/4 of the traditional PSFB dc-dc converter, leads to lower conduction losses and higher efficiencies.

Fig. 10(a) and Fig. 10(b) show the voltage oscillation and spikes on the output side of both converters. According to Fig. 10, the proposed improved PSFB charger has the lower voltage oscillation and voltage spikes, approximately 118 volts, compared with the conventional PSFB dc-dc converter leads to lower cost, lower size, and higher reliability.

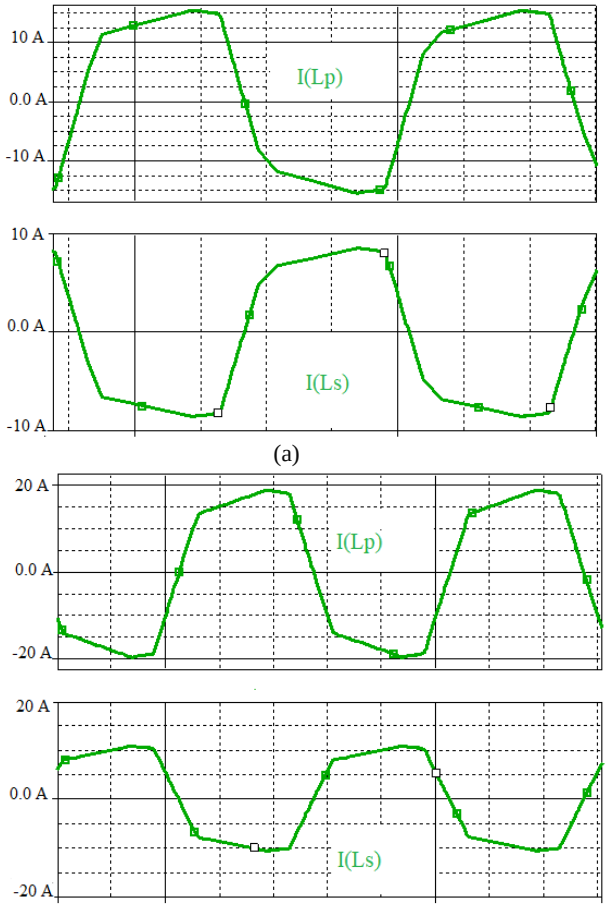


Fig. 9 The primary and secondary currents. (a) the proposed improved PSFB dc-dc converter (b) the conventional PSFB dc-dc.

In addition, the voltage spikes of the proposed improved converter for different coupling coefficients (k) are shown in Fig. 11. According to this figure, by increasing the coupling coefficient between the output filters and recursive inductors, the voltage spikes and oscillations on the secondary side will be reduced. Besides, the output voltage spikes, the primary current, and the output voltage value of both proposed improved and traditional converters for different leakage inductance are shown in Fig. 12. According to Fig. 12, by increasing the leakage inductance value, the proposed improved converter performs much better than the conventional converter. Besides, a comparison between the proposed converter and the traditional one in term of RMS currents and voltage stresses is shown in Fig. 13. This figure clearly demonstrates the major benefits of the proposed converter compared with the conventional PSFB with the CDR. The measured efficiencies in the two different conditions for both proposed improved PSFB dc-dc converter and the conventional one are listed in Table III. Besides, the measured efficiencies of

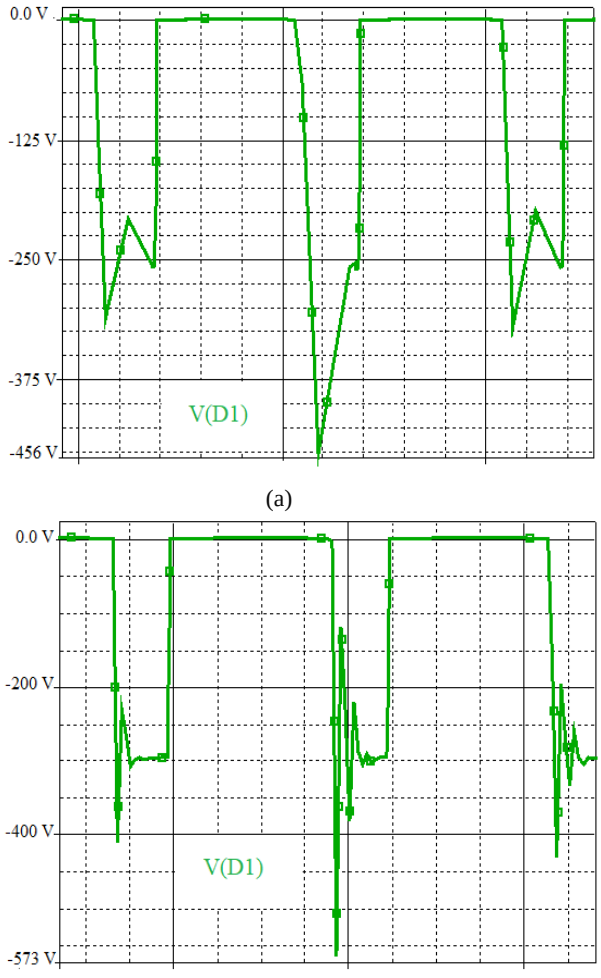
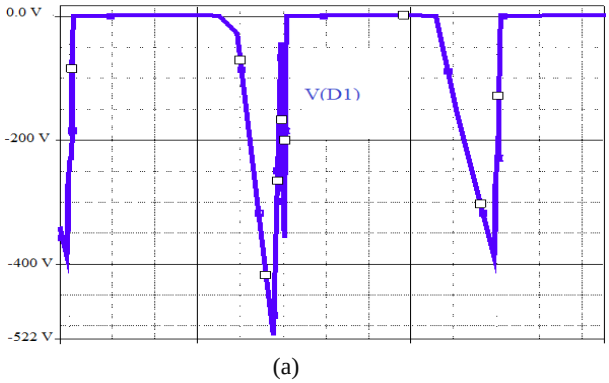


Fig. 10 The output side voltage oscillation and spikes. (a) the proposed PSFB dc-dc converter (b) the conventional PSFB dc-dc converter.

the proposed improved PSFB dc-dc converter and the traditional PSFB dc-dc converter for different loads at the nominal input voltage are shown in Fig. 14. According to this figure, the proposed converter benefits from higher efficiencies over the conventional converter for different loads. Consequently, the proposed improved PSFB dc-dc converter with two coupled inductors and the CDR is a good topology for EVs battery charger applications.



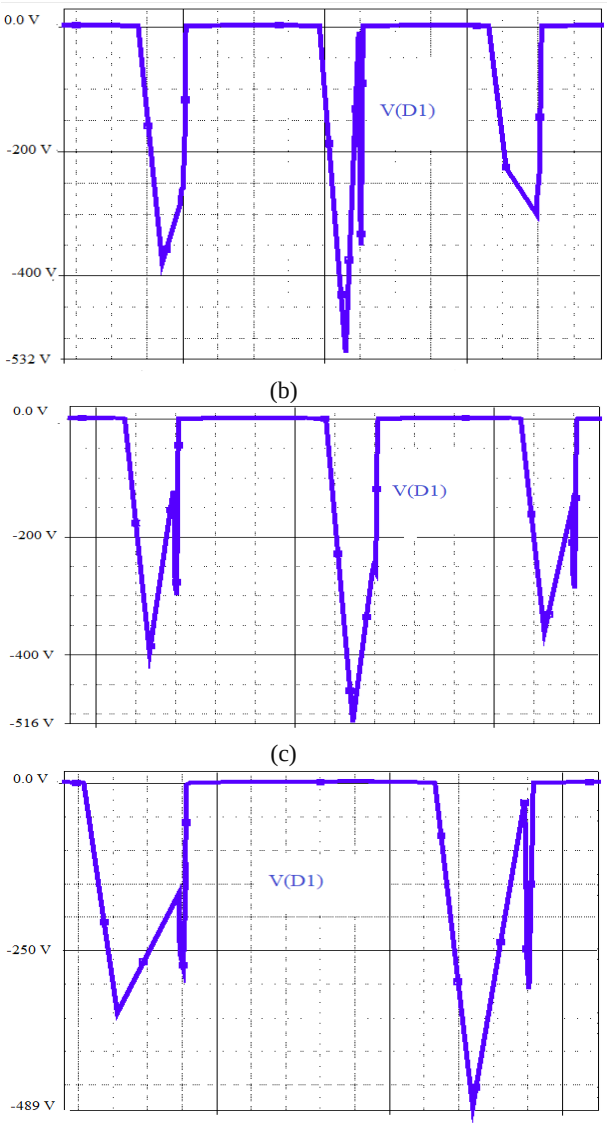
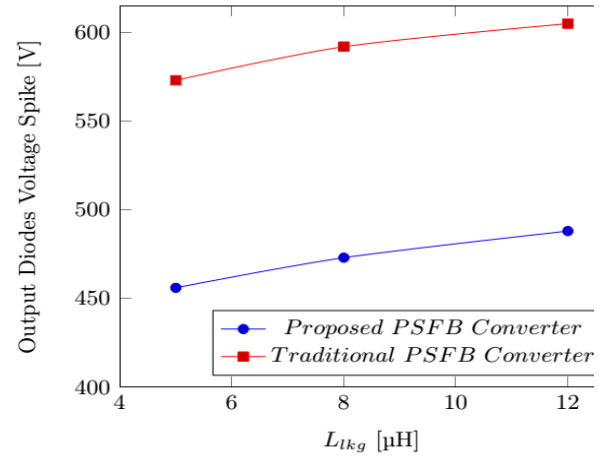
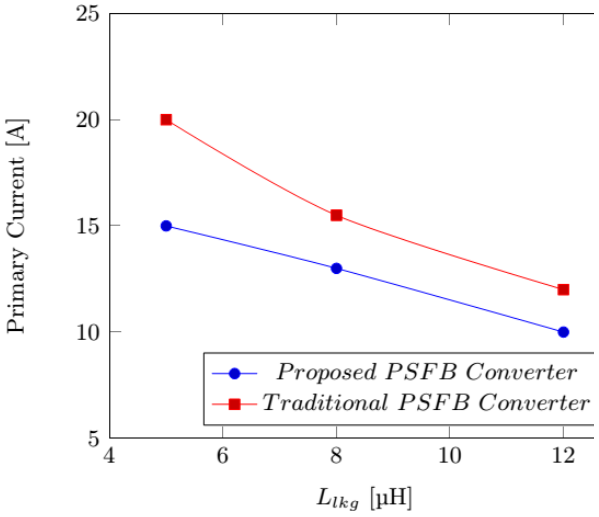


Fig. 11 The output side voltage oscillation and spikes for different coupling coefficients in the proposed improved charger. (a) k=0.005 (b) k=0.25 (c) k=0.5 (d) k=0.75.



(a)



(b)

Fig. 12 Parameters comparison between the proposed improved converter and the traditional one for different leakage inductance values. (a) the voltage spikes (b) the primary current.

Table 3 The measured efficiencies of the both proposed converter and the traditional one in two different cases.

Topology	Input Voltage	Output Power	Efficiency
The Proposed Converter	200 V	1400 W	94 %
The Traditional Converter			87 %
The Proposed Converter	250 V	140 W	92.5 %
The Traditional Converter			85 %

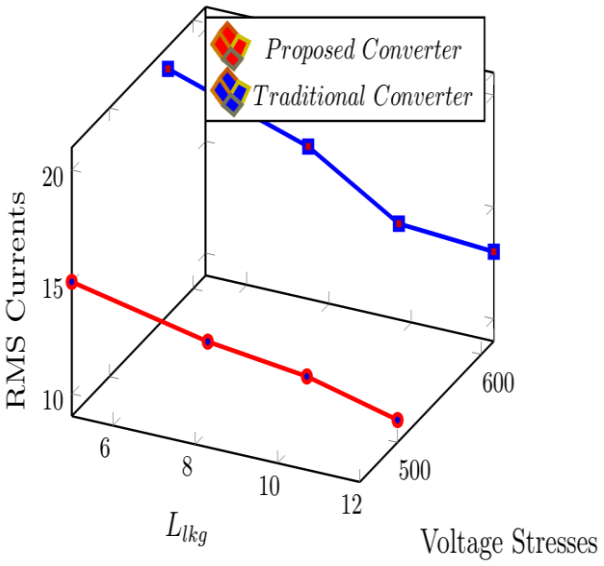


Fig. 13 RMS currents and voltage stresses comparison between the proposed converter and the traditional PSFB converter.

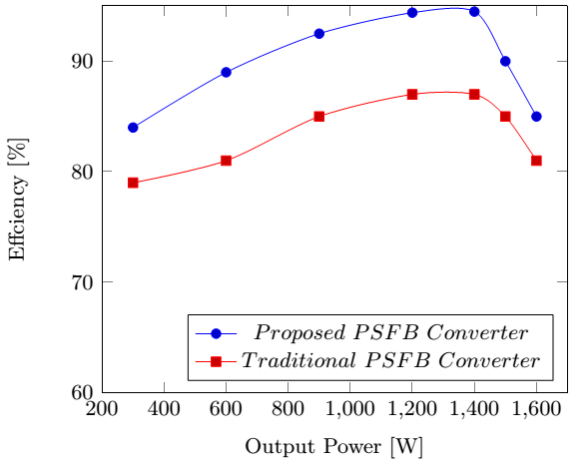


Fig. 14 Efficiencies comparison between the proposed improved converter and the traditional one for different load at the nominal input voltage.

6. Conclusion

In this study, an improved phase-shifted full-bridge dc-dc converter with two coupled inductors and a current doubler rectifier circuit for the electric vehicles battery charger applications has been proposed. The proposed improved charger has the following major benefits over the traditional PSFB with the CDR including:

- Higher efficiency because of lower RMS currents and conduction losses
- Higher reliability with the lower costs due to lower stress on the secondary side components
- Higher efficiency because of a wider ZVS operation range of power MOSFETs
- Lower circulating currents values which results in higher efficiencies

In addition, neither a complex control system nor auxiliary circuits and components in the proposed improved PSFB charger are needed. Consequently, the improved converter benefits from control simplicity and simple topology, as compared with other structures.

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